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APPLICATION FOR LETTERS PATENT

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Semiconductor Processing Methods Of Forming Transistors, Semiconductor Processing Methods Of Forming Dynamic Random Access Memory Circuitry, And Related Integrated Circuitry

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SEMICONDUCTOR PROCESSING METHODS OF FORMING TRANSISTORS, SEMICONDUCTOR PROCESSING METHODS OF FORMING DYNAMIC RANDOM ACCESS MEMORY CIRCUITRY, AND RELATED INTEGRATED CIRCUITRY

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TECHNICAL FIELD

This invention relates to semiconductor processing methods of forming transistors, to semiconductor processing methods of forming dynamic random access memory circuitry, and to related integrated circuitry.

BACKGROUND OF THE INVENTION

Semiconductor processing typically involves a number of complicated steps which include patterning, etching, and doping or implanting steps, to name just a few, which are necessary to form desired integrated circuitry. One emphasis on improving the methods through which integrated circuitry is formed, and which is directed to reducing the processing complexity, relates to reducing the number of processing steps. By reducing the number of processing steps, risks associated with processing mistakes entering into the processing flow are reduced. Additionally, wherever possible, it is also highly desirable to reduce processing complexities while providing added flexibility in the processing itself.

For example, several processing steps are required to form transistor constructions. One or more of these steps can include a

threshold voltage definition step in which one or more channel implantation steps are conducted to define the threshold voltage for the ultimately formed transistor. In some applications, it is desirable to have transistors with different threshold voltages. Typically, different threshold voltages are provided by additional masking and doping or implanting steps to adjust the doping concentration within the channel region of the various transistors desired to have the different threshold voltage. Specifically, one transistor might be masked while another receives a threshold implant; and then other of the transistors might be masked while the first-masked transistor receives a threshold implant.

This invention grew out of concerns associated with reducing the processing complexities involved in forming transistors having different threshold voltages.

SUMMARY OF THE INVENTION

Semiconductor processing methods of forming transistors, semiconductor processing methods of forming dynamic random access memory circuitry, and related integrated circuitry are described. In one embodiment, active areas are formed over a substrate, with one of the active areas having a width of less than one micron. A gate line is formed over the active areas to provide transistors having different threshold voltages. Preferably, the transistors are provided with different threshold voltages without using a separate channel implant for the

transistors. The transistor with the lower of the threshold voltages corresponds to the active area having the width less than one micron.

In another embodiment, a plurality of shallow trench isolation (STI) regions are formed within a substrate and define a plurality of active areas having widths at least some of which are no greater than about one micron, with at least two of the widths preferably being different. A gate line is formed over the respective active areas to provide individual transistors, with the transistors corresponding to the active areas having the different widths having different threshold voltages. In an STI process, devices having width smaller than 1 micron typically also have a lower threshold voltage. This is referred to as “reversed narrow width” effect as contrasted with the case of transistors formed using LOCOS isolation, where threshold voltage tends to increase as device width decreases.

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In another embodiment, two field effect transistors are fabricated having different threshold voltages without using a separate channel implant for one of the transistors versus the other.

In yet another embodiment, two series of field effect transistors are formed, with one series being isolated from adjacent devices by shallow trench isolation, the other series having active area widths greater than one micron. The one series is formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series.

In yet another embodiment, one of the two series of field effect transistors are isolated by shallow trench isolation, and different threshold voltages between the field effect transistors in different series are achieved by varying the active area widths of the field effect transistors in the series. At least one of the series preferably has active area widths less than one micron.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic side sectional view of the semiconductor wafer fragment in process in accordance with one embodiment of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 1.

Fig. 3 is a plan view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 2.

Fig. 4 is a side view of the Fig. 3 wafer fragment.

Fig. 5 is a schematic diagram of circuitry formed in accordance with another embodiment of the invention.

Fig. 6 is a schematic diagram of circuitry formed in accordance with another embodiment of the invention.

Fig. 7 is a schematic diagram of circuitry formed in accordance with another embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment in process is shown generally at 10, and includes a semiconductive substrate 12. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Referring to Fig. 2, a plurality of active areas are formed over substrate 12, with an exemplary pair of active areas 14, 16 being shown. Active areas 14, 16 can constitute individual active sub-areas within a larger active area. In a preferred embodiment, active areas or sub-areas 14, 16 are defined between a plurality of shallow trench isolation regions 18 which are received within substrate 12. The spacing of shallow

trench isolation regions 18 defines a plurality of active area widths, with exemplary widths being shown at w_1 and w_2. Preferably, at least two of the widths are different from one another. Of course, more than two of the widths could be different from one another.

In one embodiment, some of the active area widths are no greater than about one micron. One micron happens to be a break point that is technologically dependent. In other words, STI transistors show a threshold voltage reduction with reducing gate width when the gate width is about one micron or less. It will be understood that other sizes that correspond to a break point in threshold voltage versus gate width or control element size for transistors made using other technologies could be used instead of "one micron".

In one embodiment, one or both of widths w_1 and w_2 could be less than one micron. In a preferred embodiment, the different active area widths impart to transistors which are to be formed, different threshold voltages which, in a most preferred embodiment, are achieved without conducting or using a separate channel implant for the different transistors. Such results in a reduction in the number of processing steps which were previously required to form transistors having different threshold voltages.

In one embodiment, the different threshold voltages are each less than two volts. In another embodiment, the different threshold voltages are each less than one volt. In this example, the transistor having the

lower of the threshold voltages corresponds to the transistor which is formed relative to the active area having the lesser or smaller active area width.

With respect to provision of the channel implant(s) which defines the threshold voltages, one or more such implants can be conducted relative to the active areas. Preferably, each of the one or more channel implants are common to the transistors having the different active area widths which, in turn, provides transistors having different threshold voltages.

Fig. 3 is a plan view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 2, and Fig. 4 is a side view of the Fig. 3 wafer fragment. A transistor gate line 20 is formed over respective active areas 14, 16 to provide individual transistors, wherein the transistors corresponding to the active areas having the different active area widths have different threshold voltages as discussed above. Gate lines such as line 20 typically have a gate oxide layer, one or more conductive layers such as polysilicon and a silicide layer, one or more insulative caps, and insulative sidewall spacers (not shown), none of which are specifically designated. The illustrated gate line constitutes a common gate line which is formed over the illustrated active areas. It is, of course, possible to form separate gate lines over the active areas having the different widths.

Alternately considered, and in accordance with one embodiment of the present invention, two series of field effect transistors are formed over substrate 12. One of the series of field effect transistors (an exemplary transistor of which being formed over active area 14) is isolated from other adjacent devices by shallow trench isolation regions 18. The other series of field effect transistors (an exemplary transistor of which being formed over active area 16) has active area widths greater than one micron, with the first-mentioned series being formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series. Preferably, the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants. In a most preferred embodiment, the one or more common channel implants are the only implants which define the threshold voltages for the two series of field effect transistors.

Further and alternately considered, and in accordance with another embodiment of the present invention, the two series of field effect transistors just mentioned include at least one series which is isolated from adjacent devices by shallow trench isolation regions such as regions 18. Different threshold voltages are achieved between field effect transistors in the different series by varying the active area widths of the field effect transistors in the series, with at least one of the series having active area widths less than one micron, or less for future technologies.

Accordingly, field effect transistors can be fabricated having different threshold voltages without using a separate channel implant for the field effect transistors having the different threshold voltages. Such can result in a reduction in processing steps, which formerly included additional masking steps. One or more of the active areas can have widths less than one micron, with such widths being varied in order to change the threshold voltages of the transistors formed thereover.

In operation, various methods of the invention provide integrated circuitry having transistors with different threshold voltages without the added processing complexity. In a preferred embodiment, various methods of the invention can provide dynamic random access memory circuitry having a memory array area for supporting memory circuitry and a peripheral area for supporting peripheral circuitry. A plurality of shallow trench isolation regions are received within the peripheral area of the substrate and define a plurality of active areas having widths within the substrate, some of the widths being no greater than about one micron. Preferably, at least two of the widths are different. A conductive line is formed or disposed over the respective active areas to provide MOS gate electrodes for individual transistors. The transistors corresponding to the active areas having the different widths preferably have different threshold voltages. Exemplary dynamic random access memory circuitry is described in U.S. Pat. Nos. 5,702,990 and 5,686,747, which are incorporated by reference.

Referring to Fig. 5, a circuit 28 is provided and includes transistors 30, 32. Such transistors can be fabricated, in accordance with the methods described above, to have different threshold voltages. In this example, transistor 30 serves as a pass transistor and has a low threshold voltage V_{tl}, while transistor 32 serves as a switching transistor and has a high threshold voltage V_{th}.

Referring to Fig. 6, a circuit 34 is provided and includes transistors 36, 38 which can have different threshold voltages. Such circuit comprises a portion of precharge circuitry for dynamic random access memory circuitry. In the example of Fig. 6, the transistor 36 has a low threshold voltage V_{tl} and the transistor 38 has a high threshold voltage V_{th}.

Referring to Fig. 7, a circuit is shown generally at 40 and comprises transistors 42, 44 and 46 having threshold voltages V_{t1}, V_{t2} and V_{t3}, respectively. The transistors 42, 44 and 46 are fabricated to be formed in a parallel configuration with a common gate line 48 interconnecting the transistors 42, 44 and 46 and coupling a signal C_{SAL} to gates of the transistors. In this example, the transistors 42, 44, 46 each have different active area widths which results in different threshold voltages.

Also shown in Fig. 7 is a sense amplifier circuit 50 including cross-coupled transistors 52 and 54. In one embodiment, the transistors 52 and 54 are formed to have a low threshold voltage V_{tl}. When the

signal C_{SAL} goes to logic "1", the common node labeled RNL* equilibrates the potentials on sources of the transistors 52 and 54 in preparation for reading stored data from memory cells in a memory array (not shown). In the example shown in Fig. 7, the circuit 40 acts as a pull-down circuit and equilibrates the node RNL* to ground. Use of multiple transistors 42, 44 and 46 having different threshold voltages facilitates ("softens") sensing at the beginning of the sensing cycle and also more rapid sensing at the end of the cycle when differential signals have been developed by the transistors 52 and 54.

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Advantages of the invention can include provision of a plurality of transistors having different threshold voltages, without the necessity of providing different dedicated processing steps to achieve such different threshold voltages. In various preferred embodiments, such results are attained through the use of shallow trench isolation and various so-called reverse narrow width characteristics. Additionally, current drive can be achieved using multiple narrow width devices in parallel of the same or different V_t's ~~(Fig. 7)~~. The invention can be useful for low threshold voltage applications such as precharge circuitry in DRAM circuitry, or as output drivers where low threshold voltages are important to obtain higher signal levels.

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In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means

herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.